REMARKS

The Office Action dated December 9, 2006 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-23 are pending and are submitted for consideration.

Claims 1, 18, and 23 stand rejected under 35 U.S.C. §102(a) as being anticipated by *Sadjadpour* (U.S. Publication No. 2001/0055332). The Office Action took the position that *Sadjadpour* teaches each and every element recited in the rejected claims. Applicants traverse the rejection and respectfully submit that each of claims 1, 18, and 23 recite subject matter that is not taught or disclosed by *Sadjadpour*.

Independent claim 1, upon which claims 2-4, 9, and 11-14 depend, recites a communication system for transferring data between a transmitter and a receiver over a plurality of channels, the communication system comprising modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences, circuitry for determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and circuitry for selecting a bit loading sequence with a lowest error rate.

Independent claim 18 recites a method for transferring data between a transmitter and receiver over a communication channel, the method comprising identifying a set of bit loading sequences from a plurality of modulation alphabets, determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and selecting a bit loading sequence with a lowest error rate and applying the power allocation to at least one communication channel.

Independent claim 23 recites a communication system for transferring data between a transmitter and a receiver over a plurality of channels, the communication system comprising providing means for providing a modulation circuitry having a plurality of modulation alphabets and for providing a set of bit loading sequences, determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and selecting means for selecting a bit loading sequence with a lowest error rate.

Applicants submit that each of claims 1, 18, and 23 recite subject matter that is not taught or disclosed by *Sadjadpour*.

Sadjadpour teaches a discrete multi-tone modem which attempts to minimize cross talk over a twisted pair cable. At paragraph 27, *Sadjadpour* teaches a plurality of modulation alphabets and a digital modulator that generates a set of bit loading sequences using the modulation alphabet. Further, at paragraphs 33 to 44, *Sadjadpour* discloses a method for selecting a bit loading sequence with a lowest error rate. The method is accomplished by calculating the power which will be required per tone, and therefore, indirectly of cross talk occurring within the cable when a bit is added or taken away from one of the tones (modulation alphabets).

However, although the method of *Sadjadpour* teaches that the difference in power needed to transmit one additional bit in each of the modulation alphabets or similarly to subtract or remove one bit from each of the alphabets, *Sadjadpour* does not teach or disclose circuitry or methodology for determining a power allocation for at least one bit

loading sequence based on minimizing an error rate, as recited in each of claims 1, 18, and 23. The power values shown in *Sadjadpour* are determined solely on the selection of the bit loading of each of the modulation alphabets and there is no variability of the power allocation of the selected bit loading in order to minimize an error rate, as recited in Applicants' claims. Therefore, Applicants submit that each of claims 1, 18, and 23 recite limitations that are not taught or disclosed by *Sadjadpour*. Reconsideration and withdrawal of the rejection of claims 1, 18, and 23 is respectfully requested.

Claims 2-13, 19-20, and 22 stand rejected under 35 U.S.C. §103(a) as being obvious in view of *Sadjadpour* in view of *Applicants' admitted prior art.*. The Office Action took the position that *Sadjadpour* teaches each and every element recited in claims 2-13, 19-20, and 22, except for a MIMO system. However, the Office Action cites to Applicants' admitted prior art as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 2-13, 19-20, and 22.

As a preliminary matter, Applicants note that claims 2-13 depend from claim 1, which has been presented above as allowable over *Sadjadpour*. As such, Applicants submit that claims 2-13 are allowable as a result of being dependent upon an allowable base claim. Reconsideration and withdrawal of the rejection is respectfully requested.

Independent claim 19 recites a communication system for transferring data between a transmitter and receiver over a communication channel, the system comprising a first circuitry means for decomposing a communication channel into a plurality of logical channels, modulation circuitry having a plurality of modulation alphabets, at least two modulation alphabets are capable of representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels, a second circuitry means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences, and a third circuitry for choosing a bit loading sequence having a minimum bit error rate.

Independent claim 20 recites a method for transferring data between a transmitter and receiver over a communication channel, the method comprising decomposing a communication channel into a plurality of logical channels, selecting from a plurality of modulation alphabets, wherein at least two modulation alphabets for modulating data are capable of representing the data using a different number of bits, identifying a set of bit loading sequences for a fixed data rate which specify a number of bits to be loaded onto corresponding logical channels of the plurality of channels, allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences, and choosing a bit loading sequence having a minimum bit error rate.

Independent claim 22 recites a communication system for transferring data between a transmitter and receiver over a communication channel, the system comprising decomposing means for decomposing a communication channel into a plurality of logical channels, representing means for representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels, allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences, and choosing means for choosing a bit loading sequence having a minimum bit error rate.

Applicants submit that each of claims 2-13, 19-20, and 22 each recite subject matter that is not taught, disclosed, or otherwise suggested by the combination of *Sadjadpour* and Applicants' admitted prior art.

In traversing the rejection, Applicants first note that neither *Sadjadpour* nor Applicants' admitted prior art, when taken alone or in combination, teach the determining power allocation feature recited in each of the rejected claims. Therefore, Applicants submit that each of claims 2-13, 19-20, and 22 recite subject matter that is not taught, disclosed, or otherwise suggested by the cited combination of references. As such, reconsideration and withdrawal of the rejection of claims 2-13, 19-20, and 22 is respectfully requested.

Further, Applicants submit that it is well known that obviousness can only be established by combining or modifying the teachings of the prior art to produce the

claimed invention, where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves, or in the knowledge generally available to one of ordinary skill in the art. See, In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

In the instant case, the Office Action has merely stated that it would have been obvious to one of ordinary skill in the art to combine the teachins, without citing to any particular section from either of the references that illustrates that one of ordinary skill in the art would have been motivated to combine the references. Further, the Office Action has not presented any support for the conclusion that one of ordinary skill in the art would have known to combine the teaching of the references at the time the instant application was filed, other than to simply draw the unsupported conclusion that one would have known to combine the references. In response to this broad unsupported conclusion, Applicants note that M.P.E.P. §2143.01 states that the mere fact that references *can* be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. See, In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990). When the Office Action fails to provide specific motivation to combine references (more than a mere statement that it would have been obvious to combine the references), then the Federal Circuit, the Board, and the M.P.E.P are clearly aligned in taking the position that "the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed

invention." See, M.P.E.P § 2141 and Hodosh v. Block Drug Co., Inc. 786 F.2d 1136, 229 USPQ 182 (Fed. Cir. 1986).

Applicants submit that the Office Action has not cited any support from within the references themselves that supports a conclusion that the references were combinable. Further, the Office Action has not provided any support for a conclusion that the motivation to combine the references was available to one of ordinary skill in the art at the time the present application was filed. As such, Applicants submit that the references supporting the §103 rejection are not properly combinable. In view of the improper combination of the cited references, reconsideration and withdrawal of the rejection is respectfully requested.

Claims 14-17 and 21 stand rejected under 35 U.S.C. §103(a) as being obvious in view of *Sadjadpour* in view of *Kim* (US Patent Publication No. 2003/0128769). The Office Action took the position that *Sadjadpour* teaches each and every element recited in claims 14-17 and 21, except for codings and modulations that utilize system bits and parity bits. However, the Office Action cites *Kim* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 14-17 and 21.

As a preliminary matter, Applicants note that claims 14-17 and 21 each depend from claims 1 and 20, both of which have been presented above as allowable over the cited art. As such, Applicants submit that claims 14-17 and 21 are allowable as a result of being dependent upon an allowable base claim. Reconsideration and withdrawal of the rejection is respectfully requested.

In traversing the rejection, Applicants first note that neither *Sadjadpour* nor *Kim* when taken alone or in combination, teach the determining power allocation feature recited in each of the rejected claims. Therefore, Applicants submit that each of claims 14-17 and 21 recite subject matter that is not taught, disclosed, or otherwise suggested by the cited combination of references. As such, reconsideration and withdrawal of the rejection of claims 14-17 and 21 is respectfully requested. Further, as noted above with respect to the rejection of claims 2-13, 19-20, and 22, Applicants again submit that the Office Action has not properly supported the §103 rejection, as there is no teaching or suggestion found within the references that suggests the desirability of combining the teaching of the references. Applicants submit that the motivation to combine the references is only found in Applicants' disclosure, which amounts to impermissible hindsight reconstruction. Therefore, reconsideration and withdrawal of the rejection of claims 14-17 and 21 is respectfully requested.

In conclusion, Applications submit that each of claims 1-23 recite subject matter that is not taught, disclosed, or otherwise suggested by the cited prior art. Specifically, claim 1 recites circuitry for determining power allocation, and claims 18-20, 22, and 23

recite power weighting for minimizing a bit error rate of an identified bit loading sequence. Claims 1-23 are pending and are submitted for consideration.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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Enclosures: Petition for Extension of Time